[0101] FIG. **11** is a timing diagram explaining an operation of a deep standby (DSTB) mode of a display driving circuit according to some example embodiments of inventive concepts, and FIG. **12** is a block diagram explaining an operation of a deep standby (DSTB) mode of a display driving circuit according to some example embodiments of inventive concepts. For convenience in explanation, duplicate explanation of the same items as those according to the above-described embodiment will be omitted, and explanation will be made around the different point between the embodiments.

[0102] Referring to FIGS. **11** and **12**, the operating mode of the display driving circuit **1100** may be changed from the standby (STB) mode to a deep-standby (DSTB) mode. The process from the normal mode to the standby (STB) mode is the same as the contents as described above with reference to FIGS. **9** and **10**.

[0103] As the operating mode of the display driving circuit **1100** is changed from the standby (STB) mode to the deep-standby (DSTB) mode, that is, as time goes by from time tb**3** to time tb**5**, the voltage level of the second source power VDD is pulled down.

[0104] Accordingly, the input signals SD_VSP_VCISW_A, SD_VSP_VCISW_B, and SD_VSP_VCISW_C that are applied to the switch control circuit **300** may also be pulled down. However, even after the input signals SD_VSP_VCISW_A, SD_VSP_VCISW_B, and SD_VSP_VCISW_C are pulled down, the first source power VOUT that is applied to the level shift device **110** can be maintained as the second selection power VCI.

[0105] Since the second selection power VCI is continuously applied to the level shift device **110**, the output signal GND_ENH of the level shift device **110** can be maintained in an enabled state. Accordingly, the pull-down transistor **130** can be maintained in a turn-on state, and the output terminal SOUT of the operational amplifier **120** can be discharged for a sufficient time. FIG. **12** shows the operating state of the display driving circuit **1100** in the deep-standby (DSTB) mode.

[0106] Through this, the display driving circuit **1100** can discharge the plurality of pixels included in the display panel **1200** for a sufficient time.

[0107] FIG. **13** is a timing diagram explaining an operation of an abnormal mode of a display driving circuit according to some example embodiments of inventive concepts, and FIG. **14** is a block diagram explaining an operation of an abnormal mode of a display driving circuit according to some example embodiments of inventive concepts.

[0108] Referring to FIG. **13**, the operation of a display device, which operates in a normal mode, may be abnormally ended due to an unexpected error occurrence. In this case, the display driving circuit **1100** operates in an abnormal mode.

[0109] In a normal mode, the first selection power VSP is applied to the level shift device **110**, and a voltage that corresponds to image data to be output is applied to the input terminal SOUT of the display panel **1200**.

[0110] Since the second selection power VCI is a power that is input from the outside, it maintains a constant value even in a standby (STB) mode or in a deep-standby (DSTB) mode. In the case where the second selection power VCI is lowered below a reference level (desired reference value), the display driving circuit **1100** operates in an abnormal mode.

[0111] At time tc**3**, the second selection power VCI is lowered below the reference level, and the first selection power VSP and the third selection power VCI**1**, which are generated by the second selection power VCI, are pulled down together.

[0112] However, unlike the first selection power VSP, the third selection power VCI**1** is generated and output by the regulator **400**, and in an abnormal mode, the change amount of the third selection power VCI**1** may be smaller than the change amount of the first or second selection power VSP or VCI.

[0113] Specifically, referring again to FIG. **5**, the control signal CVI**1**_ABN that is input to the regulator **400** may be non-enabled in the abnormal mode, and a second transistor **404** for connecting the second node N**2** and the third node N**3** to each other may be turned off.

[0114] Then, the second node N**2** may be pulled down as the first transistor **408** is turned on, but the voltage of the third node N**3** may become equal to the voltage of the charged capacitor. That is, as the second transistor **404** is turned off, the charge that is stored in the capacitor is discharged at low speed, and the voltage that is charged in the capacitor may be continuously transferred to the third selection power VCI**1** as a floating power.

[0115] As the first selection power VSP and the second selection power VCI are pulled down, a combination of the input signals SD_VSP_VCISW_A, SD_VSP_VCISW_B, and SD_VSP_VCISW_C that are applied to the switch control circuit **300** is changed, and the voltage that is applied to the level shift device **110** is changed to the third selection power VCI**1**.

[0116] Referring again to FIGS. **13** and **14**, at time tc**3** when the operating mode of the display driving circuit **1100** is changed to the abnormal mode, the input signal GND_EN and the output signal GND_ENH of the level shift device **110** are enabled.

[0117] As the output signal GND_ENH is enabled, the pull-down transistor **130** that is gated by the output signal GND_ENH may be turned on, and the output terminal SOUT of the operational amplifier **120** may he discharged.

[0118] Then, at time tc**4**, the second source power VDD is pulled down, and thus the input signal GND_EN is also pulled down.

[0119] However, since the voltage of the third selection power VCI**1** is maintained as it is in a floated state, the output signal GDN_ENH may be maintained in an enabled state. Accordingly, the pull-down transistor **130** is maintained in a turn-on state, and the output terminal SOUT of the operational amplifier **120** is discharged in a sufficient time even in the abnormal state where the external power is not supplied. FIG. **14** shows the operating state of the display driving circuit **1100** in the abnormal state. In this case, the slope of the output signal GND ENH may be equal to the slope of the third selection power VCI**1**, but is not limited thereto.

[0120] Through this, the display driving circuit **1100** can discharge the plurality of pixels included in the display panel **1200** for a sufficient time, and can prevent the DC residual effect from occurring on the plurality of pixels. Further, it can prevent the image sticking issue from occurring on the display panel **1200**.